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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/867,064	ADILETTA ET AL.	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 and 16-26 have been examined.

2. Acknowledgement of papers filed: amendment filed on 3/14/2005.

Withdrawn Objections

3. Applicant, via amendment, has overcome the objection to the specification and title set forth in the previous Office Action. Consequently, these objections has been withdrawn by the examiner.

4. Applicant, via amendment canceling claims 12-15, has overcome the objections to claims 12-15 set forth in the previous Office Action. Consequently, these objections have been withdrawn by the examiner.

Withdrawn Rejections – 35 USC § 112

5. Applicant, via amendment canceling claim 12, has overcome the 35 U.S.C. 112, 2nd paragraph rejection to claim 12 set forth in the previous Office Action. Consequently, this rejection has been withdrawn by the examiner.

New Drawing Objection

6. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because numbers and reference characters not plain and legible, see attached Notice of Draftsperson's Patent Drawing Review. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new

drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

New Claim Rejections – 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 21 recites the limitation "each of the plurality of bits". There is insufficient antecedent basis for this limitation in the claim. It will be interpreted as "each of a plurality of bits of the self-destruct register" for the remainder of the examination.

9. Claim 23 recites the limitation "each of the plurality of bits". There is insufficient antecedent basis for this limitation in the claim. It will be interpreted as "each of a plurality of bits of the self-destruct register" for the remainder of the examination.

10. Claim 25 recites the limitation "each of the plurality of bits". There is insufficient antecedent basis for this limitation in the claim. It will be interpreted as "each of a plurality of bits of the self-destruct register" for the remainder of the examination.

11. Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 7, applicant states, "the self-destruct register automatically clears all of the bits of the self-destruct register."

However, in dependent claim 22, applicant states, "in response to a read of one or more of the plurality of bits, the self destruct register is configured to automatically clear the one or more of the plurality of bits." It is unclear whether all of the bits are cleared in the self-destruct register (as recited in claim 7), or if only certain bits are cleared, ("'automatically clear the one or more bits" from claim 22).

Maintained Claim Rejections

12. Applicant has failed to overcome the 35 U.S.C. 102 and 103 rejections set forth in the previous Office Action for claims 1-10. Therefore, these rejections are respectfully maintained by the examiner and copied below for applicant's convenience.

Maintained Claim Rejections – 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1-7, 9, 10 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Sites, U.S. Patent 5,193,167.

16. As per claim 1, a method of inter-thread communication in a multi-threaded computer (The CPUs share a memory and system bus and each can execute sequential instructions, therefore the system of Sites is multi-threaded, figure 1) comprises:

-Storing an inter-thread message in memory (address in physical address register 95), the inter-thread message having a field for an address that indicates a location of data for a next thread to execute: (CPU 10 (current thread) stores the address of data that CPU 15 (next thread) is to execute when CPU 10 executes a LDQ_L instruction (column 15, lines 6-30). Then, after CPU 15 executes a LDQ_L instruction, it will monitor CPU 10's physical address register 95 to check if there is a match, when there is a match, the address stored in physical address register 95 is also the address of data that is for CPU 15.

-And writing to a self-destruct register (lock flag 96) after storing the message (address in physical address register 95), to indicate that a thread which stored the message in memory has completed execution, with the self-destruct register configured to automatically clear upon reading: (Thread is defined as, "A single sequential flow of control within a process." (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.) The lock flag 96 is written to when the current thread executes LDQ_L, the current thread is defined as the instructions leading up to and including LDQ_L, since that is a sequential flow of control within a process. Therefore, since the lock flag 96 is set when LDQ_L is completed, and LDQ_L is the end of the current thread, it indicates that

the thread has completed execution. When the next thread executes a STQ_L instruction, the lock flag 96 is read and cleared. (Column 15, lines 5-30) Also, automatic is defined in The American Heritage College Dictionary, 4th ed. as, "2b. Acting or done as if by machine; mechanical.")

17. As per claim 2, the method of claim 1 wherein the inter-thread message field for an address provides an address of a register where the data for the next executing thread is stored (Column 15, lines 5-30; The address in physical address register 95 contains the address where the data in an operand of the next executing thread is stored. The address is for a memory location of a specified size that contains data, which by the definition in the IEEE dictionary, is a register. A register is "a storage device or storage location having a specified storage capacity." (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.)

18. As per claims 3 and 9, the method of claim 1 wherein writing to a self-destruct register further comprises: setting at least one bit in the self-destruct register which corresponds to the thread which is writing to the self-destruct register. (Column 15, lines 5-30 and figure 5; The lock flag 96 is a register that has a bit set that corresponds to the thread that is writing to it.)

19. As per claims 4 and 10, the method of claim 1 wherein writing to a self-destruct register further comprises: setting one bit in the self-destruct register which corresponds to the thread which is writing to the self-destruct register. (Column 15, lines 5-30 and figure 5; The lock flag 96 is a register that has a bit set that corresponds to the thread that is writing to it.)

20. As per claim 5, the method of claim 1 further comprising:

-Writing to the self-destruct register by a first thread (Column 15, lines 5-30; the instruction stream in CPU 10 that includes instructions leading up to and including LDQ_L is a first thread. The LDQ_L instruction writes to the lock flag 96.)

-Reading from the self-destruct register by a second thread: (Column 15, lines 5-30; the instruction stream in the CPU 15 including the STQ_L instruction is the second thread. The second thread's STQ_L instruction will read the lock flag 96)

-Where the reading further comprises: reading bits, if any, that are set in the self-destruct register; and clearing all of the bits of the self-destruct register (Column 15, lines 5-30; The lock flag 96 is read by the second thread and it is cleared afterwards)

21. As per claim 6, the method of claim 5 further comprises:

-Reading the inter-thread message from the memory by a new thread (The inter-thread message is the address stored in physical address register 95. The inter-thread message is inherently read by the new thread (the second thread) in order to monitor physical address register 95 and detect a match of addresses.)

-Where the new thread is a thread other than the first thread; and executing the new thread. (The CPUs monitor other CPUs' physical address

registers 95 to detect a match. The new thread, on CPU15, checks the other threads (other CPU's) when it is executing.)

22. As per claim 7, a hardware-based multi-threaded processor comprises:

-A general purpose processor configured to coordinate system functions (figure 1, CPU 10, it is inherent that CPU 10 coordinates system functions within CPU 10. For example, controlling the processing of instructions, including fetching, decoding, issuing and executing, is the coordinating system functions).

-A plurality of microengines configured to support multiple thread execution (Figure 1, CPU 15 and the CPU adjacent CPU 15; When each has an instruction stream, multiple thread execution is present.)

-A scratchpad memory configured to store inter-thread messages (physical address register 95) where execution of a write to the scratchpad memory by a first thread causes an address to be stored as an inter-thread message which indicates a location of data for a new thread: (CPU 10 (executes first thread) stores the address of data that CPU 15 (executes a new thread) is to execute when CPU 10 executes a LDQ_L instruction (column 15, lines 6-30) and CPU 15 executes a LDQ_L instruction after, then CPU15 will monitor CPU 10's physical address register 95 to check if there is a match, when there is a match, the address stored in physical address register 95 is also the address of data that is for CPU 15. Scratchpad memory is a temporary memory storage device, and therefore physical address register 95 is a scratchpad memory.)

-And a self-destruct register configured to indicated the execution status of threads where reading of the self-destruct register automatically clears all of the bits of the self-destruct register: (Thread is defined as, "A single sequential flow of control within a process." (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.) The lock flag 96 is written to when the first thread executes LDQ_L, the first thread is defined as the instructions leading up to and including LDQ_L. Therefore, since the lock flag 96 is set when LDQ_L is completed, and LDQ_L is the end of the first thread, it indicates that the thread has completed execution, which is the status of an executing thread. When the next thread executes a STQ_L instruction, the one and only bit of lock flag 96 is read and cleared. (Column 15, lines 5-30))

Maintained Claim Rejections – 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Sites, U.S. Patent 5,193,167 in view of Panwar, U.S. Patent 5,870,597.

25. As per claim 8, Sites teaches the processor of claim 7 wherein the plurality of microengines further comprise: executing a write to the scratchpad memory

(Physical address register 95) by the first thread to cause an address of data for a next thread to be stored.

26. However, Sites fails to teach that a first thread causes an inter-thread message that includes an address indicating the location of the register stack.

27. Panwar teaches an inter-thread message stored in Current Window Pointer (CWP) register 306 (also labeled as CWP 610 in figure 6). It is an inter-thread because multiple processes (threads) read and write to it. The address stored in the CWP register points to a window of registers (a register stack). Upon a Restore command, the CWP register is written to by the current process to indicate an address of a different process' window of registers. The CWP register is the scratchpad memory because it temporarily holds addresses and then is updated to new addresses. The process that executes the Restore command (write) is the first thread. The register window that the restored CWP register points to is for the new thread. (Column 7, line 40 to Column 8, line 5)

28. One of ordinary skill in the art at the time of the invention would have recognized that having a register window for each process allows fewer bits to be needed to address logical registers in a process. If all registers were addressable in the whole register file instead of only those within each process' window, more bits would be needed to specify an individual register. Therefore, a benefit of Panwar's register windowing is fewer bits are needed to encode instructions in order to address them in a process. For example, Panwar uses 32-register windows, and in turn, five bits are needed to address a register in a

window. Without a window, and 128 registers available as shown in figure 3, it would take 7 bits to address a specific register. (Background of the invention, columns 2 and 3). Also, one of ordinary skill in the art at the time of the invention would have recognized having one shared register file reduces the total number of registers needed, for instance, 5 processes each with 32 registers would need 160 registers, while Panwar implements a smaller, shared 128-register register file. Sites implements multiple register files for each CPU, 64 registers for each CPU, 32 for the execution unit and 32 for the floating-point unit (column 7, lines 20-28 and column 8, lines 55-61). With multiple CPUs, the amount of registers increases and becomes more costly in terms of money and chip space. One of ordinary skill in the art at the time of the invention would have recognized a shared register file would reduce the cost and size of the register file in the computer system and windowing in the shared register file would reduce the size of addresses for the register file to the amount needed to access only those in the window, thus preventing the increase in the instruction and program size.

29. It would have been obvious to combine the shared register file with register windows of Panwar and the computer system of Sites in order to reduce the cost and size of the register file hardware. This benefit would have provided motivation to one of ordinary skill in the art to combine the inventions.

New Claim Rejections – 35 USC § 102

30. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

31. Claims 1, 7, 16-21, and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Chastain et al., U.S. Patent 5,159,686, herein referred to as Chastain..

32. As per claim 1, Chastain teaches a method of inter-thread communication in a multi-threaded computer comprises:

-Storing an inter-thread message in memory, the inter-thread message having a field for an address that indicates a location of data for a next thread to execute: (Column 5, line 30-45 and column 8, lines 6-40. The fork.PC is an address within an inter-thread message (fork block) stored in memory (communication registers 46).

-And writing to a self-destruct register (semaphores 48) after storing the message to indicate that a thread which stored the message in memory has completed execution, with the self-destruct register configured to automatically clear upon reading: (Column 5, lines 9-63, column 8, lines 6-46. After the message is stored, the "forkposted" semaphore is set. Other processors are constantly polling the forkposted semaphores to see if there is a message stored,

indicating a thread for them to execute, and as indicated by column 4, lines 35-45, the semaphores are automatically cleared upon reading. Automatic is defined in The American Heritage College Dictionary, 4th ed. as, "2b. Acting or done as if by machine; mechanical." The method of Chastain, including reading and clearing the semaphores, is performed by a machine (a computer), therefore, each step is automatic.)

33. As per claim 7, a hardware-based multi-threaded processor comprises:

-A general purpose processor configured to coordinate system functions (Processor 24 is a processor that is not idle and is inviting idle processors to execute a new thread, column 5, lines 9-68)

-A plurality of microengines configured to support multiple thread execution (Figure 1, Column 4, lines 4-13, each processor in the multiprocessor system is a microengine)

-A scratchpad memory configured to store inter-thread messages where execution of a write to the scratchpad memory by a first thread causes an address to be stored as an inter-thread message which indicates a location of data for a new thread: (Column 5, line 30-45 and column 8, lines 6-40. The fork.PC is an address within an inter-thread message (fork block) stored in memory (communication registers 46).

-And a self-destruct register configured to indicate the execution status of threads where reading of the self-destruct register automatically clears all of the

bits of the self-destruct register: (Associated Semaphore, "forkposted", is cleared upon reading, and indicates the execution status of the thread (it indicates the thread is ready to be executed). If the semaphore is set, it clears upon a read, therefore, all of the bits are cleared upon a read. (Column 4, lines 36-50, and column 5, lines 9-68).

34. As per claim 16, Chastain teaches the processor of claim 7, wherein the read from the self-destruct register by the thread causes execution of a new thread for each bit that is set, if any, in the self destruct register. (A read of the self-destruct register (a forkposted semaphore) indicates a thread is waiting to be executed, and upon a processor reading a set forkposted semaphore, a new thread is executed. (Column 5, line 9-68 and column 8, lines 32-46)

35. As per claim 17, Chastain teaches a computer program product residing on a computer readable medium, the computer program product including instruction to cause one or more machines to perform operations comprising:

-Storing an inter-thread message in memory: (Column 5, line 30-45 and column 8, lines 6-40. The fork.PC is an address within an inter-thread message (fork block) stored in memory (communication registers 46).

-And setting at least one bit in a self-destruct register in response to storing the inter-thread message in a memory, the self-destruct register configured to automatically clear the at least one bit in response to a read of the at least one bit: (Column 5, lines 9-63, column 8, lines 6-46. After the message is stored, the "forkposted" semaphore is set. Other processors are constantly

polling the forkposted semaphores to see if there is a message stored, indicating a thread for them to execute, and as indicated by column 4, lines 35-45, the semaphores are automatically cleared upon reading. Automatic is defined in The American Heritage College Dictionary, 4th ed. as, "2b. Acting or done as if by machine; mechanical." The method of Chastain, including reading and clearing the semaphores, is performed by a machine (a computer), therefore, each step is automatic.)

36. As per claim 18, the computer program of claim 17, wherein the operations further comprise:

-Storing a register address as the inter-thread message in memory. (Column 5, line 30-45 and column 8, lines 6-40. The fork.PC is a register address within an inter-thread message (fork block) stored in memory (communication registers 46). Register is defined as, "A device capable of retaining information, often that contained in a small subset (for example, one word), of the aggregate information in a digital computer." (The Authoritative Dictionary of IEEE Standards Terms, 7th ed.))

37. As per claim 19, the computer program of claim 17, wherein the operations further comprise:

-Reading the contents of the self-destruct register, the reading automatically clearing the self-destruct register: (Column 5, lines 9-63, column 8, lines 6-46. After the message is stored, the "forkposted" semaphore is set. Other processors are constantly polling the forkposted

semaphores to see if there is a message stored, indicating a thread for them to execute, and as indicated by column 4, lines 35-45, the semaphores are automatically cleared upon reading. Automatic is defined in The American Heritage College Dictionary, 4th ed. as, "2b. Acting or done as if by machine; mechanical." The method of Chastain, including reading and clearing the semaphores, is performed by a machine (a computer), therefore, each step is automatic.)

-And executing a new thread according to any bits set in the self destruct register: (Each of the forkposted semaphores in the self destruct register indicates that a parallel thread is ready to be executed. (Column 5, lines 9-63, column 8, lines 6-46)).

38. As per claim 20, Chastain teaches the method of claim 1, wherein the self destruct register includes a plurality of bits, and wherein, in response to a read of one or more of the plurality of bits, the self destruct register is configured to automatically clear the one or more of the plurality of bits: (Figure 1 and column 5, lines 9-63, column 8, lines 6-46, teaches that there are a plurality of forkposted semaphores within the associated semaphores 48 (self-destruct register). Column 4, lines 35-45, teaches the semaphores are automatically cleared upon reading. Automatic is defined in The American Heritage College Dictionary, 4th ed. as, "2b. Acting or done as if by machine; mechanical." The method of Chastain, including reading and clearing the semaphores, is performed by a machine (a computer), therefore, each step is automatic.).

39. Given the similarities between claim 20 and claim 24, the arguments as stated for the rejection of claim 20 also apply to claim 24.

40. As per claim 21, Chastain teaches the method of claim 1, wherein each of a plurality of bits is associated with one of a plurality of threads: (Each of the forkposted semaphores indicates that a parallel thread is ready to be executed. (Column 5, lines 9-63, column 8, lines 6-46)).

41. Given the similarities between claim 21 and claim 25, the arguments as stated for the rejection of claim 21 also apply to claim 25.

New Claim Rejections – 35 USC § 103

42. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

43. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chastain et al., U.S. Patent 5,159,686, herein referred to as Chastain, in view of Lee et al., U.S. Patent 5,367,678, herein referred to as Lee.

44. As per claim 22, Chastain teaches the method of claim 7, wherein the self destruct register includes a bit, and wherein, in response to a read of one bit, the self destruct register is configured to automatically clear the one bit: (Figure 1 and column 5, lines 9-63, column 8, lines 6-46, Column 4, lines 35-45, teaches

the semaphores are automatically cleared upon reading. Automatic is defined in The American Heritage College Dictionary, 4th ed. as, "2b. Acting or done as if by machine; mechanical." The method of Chastain, including reading and clearing the semaphores, is performed by a machine (a computer), therefore, each step is automatic. Chastain teaches wherein in response to a read of one bit of the self destruct register, the self destruct register is configured to automatically clear.

45. However, Chastain fails to teach wherein the forkposted semaphore (self destruct register) is a plurality of bits.

46. Lee teaches wherein each processor of a multithreaded/multiprocessor system has it's own signal to specifically indicate to a processor that it should execute a thread, not the other processors. This allows specifying a transaction schedule and reducing bus contention. One of ordinary skill would also have recognized that specifying a specific processor would allow a programmer to exploit special features of different processors. For instance, specifying a processor that is better at digital signal processing (dsp) to do a dsp task would provide improved processing of the task.

47. It would have been obvious to one or ordinary skill in the art to add a bit for each processor, as Lee teaches, in the self-destruct register. This would allow the parallel multiprocessor system of Chastain to specify a transaction schedule and reduce bus contention.

48. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to increase the size of the forkposted semaphore (self destruct register) from one bit to a plurality of bits since it has been held that a difference in size is not a matter of invention and that a change in size is obvious. *In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955).*

49. As per claim 23, Chastain teaches the method of claim 7, wherein each of a plurality of bits is associated with one of a plurality of threads: (Each of the forkposted semaphores indicates that a parallel thread is ready to be executed. However, each forkposted semaphore is one bit and indicates to all idle processors that a task is waiting. (Column 5, lines 9-63, column 8, lines 6-46)).

50. Lee teaches wherein each processor of a multithreaded/multiprocessor system has it's own signal to specifically indicate to a processor that it should execute a thread, and not the other processors. This allows specifying a transaction schedule and reducing bus contention. One of ordinary skill would also have recognized that specifying a specific processor would allow a programmer to exploit special features of different processors. For instance, specifying a processor that is better at digital signal processing (dsp) to do a dsp task would provide improved processing of the task.

51. It would have been obvious to one or ordinary skill in the art to add a bit for each processor, as Lee teaches, in the self-destruct register. This would allow the parallel multiprocessor system of Chastain to specify a transaction schedule and reduce bus contention. As one of ordinary skill would have recognized, this would also allow a programmer to exploit special processing

features of processors by specifying tasks to be carried out by specific processors that are geared for the task.

Response to Arguments

52. Applicants arguments filed on 3/14/2005 have been fully considered but they are not persuasive.

53. Applicant argues the novelty/rejection of claims 1, 7-10, and 16-26.

> "the self-destruct register is 'configured to automatically clear upon reading.' This feature is neither taught or suggested in Sites."
>
> "Sites merely teaches that the lock flag 96 is set to zero, or cleared."
>
> "Sites does not teach or suggest that lock flag 96 is automatically cleared upon reading, as recited in claim 1. In fact, the language 'set to zero' implies that action is taken to clear the flag (to set it to zero)."

54. These arguments are not found persuasive for the following reasons:

a. Examiner points to column 15, lines 6-30, where Stiles does teach that the register is configured to automatically clear upon a read. Upon a read of the flag, if it is set to one, it is cleared. Applicant admits that "the lock flag 96 is set to zero, or cleared," this occurs upon a read if the flag is set to one, which is an automatic action. Automatic is defined in The American Heritage College Dictionary, 4th ed. as, "2b. Acting or done as if by machine; mechanical." The method of Stiles is performed by a machine (a computer), therefore, each step is automatic. Applicant argues the language 'set to zero' implies action is taken to clear the flag (to set it to zero)', however there is no limitation in the claim that states

that the "set to zero" taught in Sites is not automatic, the limitation 'configured to automatically clear' does not distinguish applicant's claimed invention from Sites' teachings.

55. Applicant further argues the novelty/rejection of claims 1, 7-10, and 16-26

> "The language in Sites does not teach that the lock flag 96 is configured differently than a typical flag. Lock flag 96 is clearly configured so that it may be cleared by external action other than a read of its contents."

56. Examiner points to the claim language of claims 1, 7 and 17, there is no limitation requiring that the self-destruct register cannot be cleared by external action, it is only stated that the self-destruct register is configured to automatically clear upon reading. The limitation to "automatically clear" is not inherently different than the action taken by typical flags to clear. It is also not equivalent to a flag not "being cleared by external action other than a read of it's contents". Automatic is defined in The American Heritage College Dictionary, 4th ed. as, "2b. Acting or done as if by machine; mechanical." The method of Stiles is performed by a machine (a computer), therefore, each step is automatic

Conclusion

57. **THIS ACTION IS MADE FINAL.** It is noted that new grounds of rejections for claims 1 and 7 were necessitated by newly added claims 20-21,and 22-23, all other rejections were maintained as specified above, and therefore this action is made final. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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